IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of: **OKADA, Teruo, et al.**

Group Art Unit: **2836**

Serial No.: **10/775,216**

Examiner: **Adi AMRANY**

Filed: **February 11, 2004**

P.T.O. Confirmation No.: **9967**

For: **POWER SOURCE APPARATUS SUPPLYING MULTIPLE OUTPUTS**

BRIEF ON APPEAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Docket: **040057**

Date of This Paper: **July 29, 2008**

Sir:

A Notice of Appeal was filed on May 9, 2008. The Appellant appeals from the Final Office Action dated February 12, 2008. The claims were amended on May 9 to correct a typographic error in line 10 of claim 29, concurrently with filing of the Notice of Appeal.

In the event that this paper is not timely filed, the Appellants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper to **Deposit Account No. 01-2340.**

I. REAL PARTY IN INTEREST

The real party in interest is Taiyo Yuden Company, Ltd., 16-20, Ueno 6-chome, Taito-ku, Tokyo, Japan.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-28 are canceled and claims 29-38 are pending, rejected, and appealed. Claims 29, 35, and 36 are independent.

IV. STATUS OF AMENDMENTS

The claims were amended on May 9, 2008, to correct a typographic error in line 10 of claim 29. The Examiner is assumed to have entered this amendment.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Claim 29. The Appellant explains the subject matter of claim 29 by reference to exemplary disclosure:

A multiple output power source apparatus comprising a plurality of power source circuits individually generating a plurality of DC voltages .... The right side of Fig. 1 exemplifies this feature, with four different voltages being produced.

... each of the plurality of power source circuits being equipped with an independent output control circuit ... Fig. 1 shows control circuits 200-1, 200-2, 200-3, and 200-4 for the respective voltages 5.0 V, 10 V, 2.5 V, and 1.8 V. These are described at page 4, lines 7-15 in the specification.

wherein each of the output control circuits respectively comprises: a shutdown circuit that detects an abnormality of own power source circuit to output an abnormality signal ... Fig. 1 shows that several of the power source circuits have an "HLT" terminal, which is explained at page 4, lines 27-29 as an abbreviation of "Halt" or "Fault," and also explains that the HLT terminal outputs an abnormality signal.

... *to* [1] *output an abnormality signal to output control circuits of one or a plurality of other power source circuits selected from the plurality of power source circuits via a first terminal, and* [2] *inputting an abnormality signal outputted from the output control circuits of one or a plurality of other power source circuits via the first terminal* ... The HLT terminals not only output an abnormality signal when a fault occurs in that same circuit but also accept such signals from the others; see page 4, line 29 to page 5, line 3. Fig. 2 shows that one of the control circuits (200-1) has an Abnormality Detection Circuit 205, mentioned at page 7, line 29.

... *to shut down the own power source circuit when an abnormality is detected either in the own power source circuit or in the other power source circuits*... The word "or" in this clause is discussed below.

... each of the output control circuits being operably coupled to each other, whereby the own power source circuit and the other power source circuits simultaneously shut down when an abnormality is detected either in the own power source circuit or in the other power source circuits. The word "or" occurs here also. This feature is supported at page 5, line 17: "If an abnormality is detected in one of those voltage-up-down control circuit 200-1, voltage-up control circuit 200-2, and voltage-down control circuit 200-3, other power source circuits are shut down."

The paragraph starting at page 7, line 26, states that when detection circuit 205 of control circuit 200-1 outputs an abnormality signal (Fig. 2), the abnormality signal is posted to the other power source circuits and also to the oscillator 201, so that "the own" power source is also shut down.

The shut-downs are "simultaneous;" this feature was added by an amendment.

The other circuits are similar (page 8, lines 3-6).

Independent Claims 33, 35, 36. Each of these independent claims recites the simultaneous shutdown feature discussed above, and is supported by the same disclosure; below, all of these claims are argued for on the same basis as claim 29. In addition, these claims recites master and slave circuits, illustrated in Figs. 4 and 6 (Fig. 4 is a variation on Fig. 1, see page 9, lines 29-30). The specification at page 10, line 25 to page 11, line 4 describes that the circuits of Fig. 4 are operated with synchronous oscillation.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(1) Claims 33, 35, and 36 are rejected under 35 USC § 112, second paragraph (¶¶ 2-3 on page 3 of the Action).

(2) Claims 29-34, 36, and 38 are rejected as obvious under 35 USC § 103(a) over Tominaga US 5,237,208 in view of Takahashi US 5,768,117 and Prager US 5,875,104.

(3) Claims 29-32, 35, and 37 are rejected as obvious under 35 USC § 103(a) over Tominaga, Takahashi, Prager, and further in view of Luo US 2005/0073783.

VII. ARGUMENT AGAINST REJECTION OF CLAIMS 33, 35, & 36 under 35 U.S.C. § 112, Second Paragraph

This rejection is made over the amendment of January 14, 2008, reciting in the rejected claims that "the own power source circuit and the other power source circuits simultaneously shut down and the master power source circuit and the slave power source circuit synchronously oscillate when an abnormality is detected either in the own power source circuit or in the other power source circuits." The Examiner asserts that "the claim is indefinite because it does not indicate how the master and slaves can operate after they are turned off," and the Examiner rejects claims 33, 35, and 36 under § 112, second paragraph as indefinite.

The Examiner presupposes that "shut down" in the claims means complete de-energizing of the entire unit, so that if one part becomes inoperative then all other parts must also become inoperative. For example, in the Appellant's Fig. 2, the Examiner would suppose that if drive circuit 204 becomes inoperative, then oscillator 201 must also. However, such a limitation is not found either in the claims or in the supporting disclosure. In Fig. 2, power comes from Vcc at upper left, and this power does not reach the oscillator 201 through the drive circuit 204; they are powered in parallel. The oscillator 201 is powerable independently of the drive circuit 204, according to Fig. 2. Thus, even if circuit 204 were completely de-energized when it were shut down (there is no support for this assumption), the oscillator 201 could still work.

If the claim recites that the master and slave circuits oscillate while the power source circuits do not output their voltages, then there is no impossibility. (It is noted that none is asserted, as there is no rejection under § 101.)

With respect, there is no lack of definiteness. To state that one thing is powered, and another is not, or that one operates and the other does not, is perfectly definite.

VII. ARGUMENT AGAINST REJECTION OF CLAIMS 29-34, 36, & 38 under 35 U.S.C. § 103(a)

Plural Voltages. The Examiner admits (bottom of page 4) that Tominaga does not disclose the claimed feature of *a plurality of power source circuits individually generating a plurality of DC voltages,* and relies on Takahashi. The Examiner asserts —incorrectly—that Takahashi's power source circuits con1 to con4 individually generate a plurality of DC voltages (page 5, line 1). The Examiner assertion cannot possibly be correct, because the power source circuits are connected in parallel (Fig. 1) to a "common bus ... having a *predetermined* voltage" (col. 2, lines 37-39; emphasis added). The Examiner's assertion is physically impossible.

Prager, like Takahashi, also fails to disclose different voltages. At col. 3, line 64, Prager states that the converters 101a-103a "share equally in delivering power to the load," and they are connected to the load in parallel; this implies that all have the same voltage.

The Word "Or" and Simultaneous Shutdown. The Examiner had stated in the first action at page 2, lines 3-6 of ¶ 1, that "or" was interpreted as an exclusive "or" rather than a logical "or," and had applied this interpretation to support the rejection. The Appellant had replied that the Examiner's interpretation was contrary to the true meaning, arguing:

> The word "or" is often used informally with mutually exclusive conditions (such as "either it is or it isn't") but in such cases both conditions *cannot* occur. When "or" is used with *non*-exclusive conditions (as in "If either I get a raise or my rent goes down, I'll go on vacation") then the result follows from either one of the conditions *or both* ("I got a raise *and* my rent went down—I'm going on vacation!") The Examiner is invited to consider the "or" of formal logic, and the digital OR truth table.[1]

The Examiner replied in the final Action (page 2, line 4), "the non-exclusive example provided by applicants still allows for a YES/HIGH output when only one condition is met (my rent went

[1] In logic, if a condition follows from "A or B," then it also follows from both of A and B. That is, (A or B) is true if A is true, B is true, or both A and B are true.

down, I did not get a raise, but I will still go on vacation). This argument is made moot by the claim amendments which require 'simultaneous shutdown' in more than one power source."

With respect, the Examiner confuses the premises (conditions) of a logical statement with the conclusion of a logical statement. In stating that "This argument is made moot by the claim amendments which require 'simultaneous shutdown' in more than one power source," the Examiner addresses only the *conclusion*. The claim states that there is a simultaneous shutdown "when [condition A] or [condition B]," which as a logical syllogism would read, "if A or B, then simultaneous shutdown."

It is the relation of the two conditions (premises) that are at issue, not the result—the truth table does not change if the outcome changes. That is, "If A or B, then C" has exactly the same truth table as "If A or B, then D."

The Appellant's previous argument is still valid.

Takahashi. The Examiner also admits that the primary reference Tominaga does not disclose the feature at issue in the "or" discussion above, namely, *the own power source circuit and the other power source circuits simultaneously shut down when an abnormality is detected either in the own power source circuit or in the other power source circuits*. The Examiner relies on Takahashi for disclosing this feature, but provides no citation.

Contrary to the Examiner's un-supported assertion, Takahashi does <u>*not*</u> disclose simultaneous shutdown due to an abnormality: The honorable Board is invited to consider:

(1) Takahashi's circuits include portions, labeled as "CONT" for "control" (col. 4, line 51), which are interconnected (Fig. 1). According to Takahashi (col. 5, line 10), "the largest current value [output current] among the plural converters appears in the control line CL. Accordingly, each converter is controlled to output a current having a magnitude that is equal to the largest current value." From this it follows that a failure of one circuit to produce current will not shut down the others; they will ignore such an abnormality, contrary to the Appellants' claim language, because it is lower than the others.

Takahashi states this explicitly at, e.g., col. 5, line 22: "if a converter fails, it is necessary to maintain consistent the operation of the remaining converters .... the current value does not decrease."

Furthermore, the first-listed object of Takahashi is to provide "a stable output power supply, without being affected by a failed converter." Thus, Takahashi not only fails to disclose the Appellants' feature but also teaches directly opposite to it.

(2) If, on the other hand, the current increases abnormally in one converter, the others will try to follow it, because they seek the "magnitude that is equal to the largest current value." In this case they will all overheat, rather than all shut down.

(3) The text cited by the Examiner at col. 7, lines 6-11 does not at all support the rejection.

(4) The Examiner states (last paragraph on page 5), "Takahashi [allows] only one circuit to fail (col. 12, lines 7-18). Takahashi, however, does not expressly state the outcome of exceeding the allowance failure number." With respect, the Examiner's statement and the cited text both appear to be irrelevant to the issues, and the relationship between one failure and a failure number is unclear; is the failure number one? The Appellants submit that this portion of the rejection needs to be clarified before it should be given any weight.

Prager. The Examiner also relies on Prager for disclosing the Appellants' simultaneous shutdown feature (apparently as an alternative to Takahashi). Prager is similar to Takahashi in that it attempts to have all the converters work equally hard (col. 3, line 63 to col. 4, line 4).

The Examiner states that Fig. 1 discloses a shut-down circuit, apparently referring to element 200 that is connected to the converter modules 101-103 in Fig. 1, that are mentioned in the rejection. The reference itself refers to element 200 as a "phased array controller" (col. 5, line 5) and states that it does *not* shut down all the converter modules when there is a fault. The reference states: "If one or more individual converters should fail during operation, the controller 200 will disconnect the failed converters ... and phase stagger the conversion cycles of the remaining *active* converters" (col. 5, lines 28-34; emphasis added). This passage is in the

text applied by the Examiner (col.11, lines 29-57), but it discloses the *opposite* of what the claim recites: the other converters remain "active."

None of the references discloses the Appellants' feature of simultaneous shutdown. Therefore, no combination of the applied references (not admitted) could reach the instant claims.

Non-Applied Reference. At page 2, third paragraph, the Examiner remarks that the Prager and D'Atre references disclose simultaneous shutdown. The Examiner's remark is wrong as to Prager, and improper as to D'Atre because D'Atre is not applied in the rejection. There is no citation to D'Atre.

Different Rejection. Claims 29-32 are rejected as discussed above, but are also rejected over the same references with the additional of a fourth reference, Luo. The second rejection implies that the first rejection is inadequate, for lacking Luo.

Combination. The asserted combination has no expectation of success, because the references are incompatible. The uninterruptible power supply of Tominaga outputs AC, while Takahashi outputs DC, and Prager discloses yet a third kind of output, pulses. The outputs of the three references are mutually incompatible, and therefore these references cannot be combined without destroying the function of two of them; there is no expectation of success. Furthermore, the person of ordinary skill would not have even tried to combine them because they inherently teach against combination. Changing any one to have the output of another would make it useless for its intended purpose, namely, supplying a particular form of power.

Terminal. The Examiner asserts (top of page 3) that "The use of 'a terminal' ... does <u>not</u> require that this terminal be the <u>same</u> as the terminal." The Examiner appears to assert that the Appellants' claimed first terminal is really *two different* terminals. The Examiner's assertion is understood to be analogous to asserting that "a door for going in and out" must really be a recitation "one door for going in and another, different door for going out." This is respectfully traversed as contrary to logic and claim construction (the honorable Board is invited to note that the Appellant recites a second terminal in a dependent claim).

Claim 31. Tominaga describes a configuration in which, during the an inverter mode operation, oscillating circuit trigger pulse phases in all of the triport UPS's are made coincident to each other by the parallel synchronizing signal generating circuit 41, to substantially nullify any deviation of synchronization error among the inverters or any difference in phase among the output voltages. Therefore the circulating current is minimized by conforming the phases of the oscillating circuit trigger pulses in all of the triport UPS's by the parallel synchronizing signal generating circuit.

On the other hand, the Appellants describe a configuration in which synchronous oscillations are conducted between power source circuits connected by CLK terminals for the purpose of optimizing the efficiency by setting the optimum oscillating frequency for each output voltage, both to optimize efficiency and for the purpose of suppressing the generation of beat noise, etc. According, the present invention is totally different from Tominaga in configuration and purpose.

Dependent Claims. The other dependent claims are patentable by their dependence.

VII. ARGUMENT AGAINST REJECTION OF CLAIMS 29-32, 35, & 37 under 35 U.S.C. § 103(a)

The Appellants argued above that the first three references all fail to disclose a basic feature of claim 29, namely, that all shut down simultaneously when one shuts down. Now the Appellants point out that the tertiary reference, Luo, also fails to disclose this feature.

Luo. Luo, like Tominaga, discloses an uninterruptible power supply ("UPS") with UPS modules "(10)(101-10N)" (see Fig. 1). Its object is "controlling current sharing. When the power system experiences abnormal situations ... the gain value of the controller is instantly adjusted" (paragraph 0008). That is, the goal is for the output to be stable, not to be shut down (hence the term "uninterruptible").

Paragraph 0081 of Luo states, "The high reliability of the parallel power system is because many UPS modules are collectively operated to supply power to the load. Such a high reliability is based on the assumption that even when the power system has the problem single point failure, the parallel power system will still work for the load requirement." That is, if any one UPS fails, the others will continue to output power. This is directly contrary to the Appellants' claim.

As with the first rejection, no combination of the references, even if combined (not admitted), could possible reach the claims.

None of the references discloses the Appellants' feature of simultaneous shutdown. Therefore, no combination of the applied references (not admitted) could reach the instant claims.

Dependent Claims. The dependent claims are patentable by their dependence.

In summary, not one of the applied references actually discloses the Appellants' feature of simultaneous shutdown. The Examiner is, with respect, mistaken.

For the reasons above, the honorable Board is requested to overturn the rejections.

Respectfully submitted,

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CLAIMS APPENDIX

Claims 1 - 28 (Canceled)

Claim 29 (Previously Presented): A multiple output power source apparatus comprising a plurality of power source circuits individually generating a plurality of DC voltages, each of the plurality of power source circuits being equipped with an independent output control circuit, wherein

each of the output control circuits respectively comprises:

a shutdown circuit that detects an abnormality of own power source circuit to output an abnormality signal to output control circuits of one or a plurality of other power source circuits selected from the plurality of power source circuits via a first terminal, and inputting an abnormality signal outputted from the output control circuits of one or a plurality of other power source circuits via the first terminal to shut down the own power source circuit when an abnormality is detected either in the own power source circuit or in the other power source circuits, each of the output control circuits being operably coupled to each other, whereby the own power source circuit and the other power source circuits simultaneously shut down when an abnormality is detected either in the own power source circuit or in the other power source circuits.

Claim 30 (Previously Presented): The multiple output power source apparatus according to claim 29, wherein

the plurality of power source circuits respectively comprises a converter that is driven by a switching circuit, converts an input voltage into a prescribed output voltage, and outputs the prescribed output voltage, and

the output control circuits respectively comprises an output stabilizing circuit that stabilizes the output voltage of the converter of the own power source circuit by monitoring the output voltage of the converter and controlling the switching signal.

Claim 31 (Previously Presented): The multiple output power source apparatus according to claim 30, wherein the output stabilizing circuit comprises:

a reference voltage generating circuit that generates a prescribed reference voltage;

an output voltage monitoring circuit that monitors the output voltage of the converter based on the reference voltage generated by the reference voltage generating circuit;

an oscillator that generates a clock signal having a prescribed frequency;

a driving circuit that controls the clock signal generated by the oscillator based on the monitored output of the voltage monitoring circuit to stabilize the output voltage of the power source circuit to a prescribed value, and

the shutdown circuit comprises:

an abnormality detecting circuit that is connected to a first terminal of the other power source circuits, outputs an abnormality signal to the first terminal when an abnormality of the own power source circuit is detected, inputs an abnormality signal outputted from the output control circuits of the other power source circuits, and stops oscillation of the oscillator when an abnormality of the own power source circuit is detected or when the abnormality is inputted from the output control circuits of the other power source circuits.

Claim 32 (Previously Presented): The multiple output power source apparatus according to claim 29, wherein one of the plurality of power source circuits is set as a master power source circuit and one or the plurality of the power source circuits except the master power source circuit is set as a slave power source circuit, an oscillator in an output circuit of the master power source circuit of the plurality of the power source circuits is connected to an output circuit of the slave power source circuit selected from the plurality of the power source circuits via a second terminal, and outputs a synchronous oscillation signal synchronized with the clock signal via the second terminal, and

an oscillator in an output control circuit of the slave power source circuit is connected to the output circuit of the master power source circuit via a third terminal, and inputs the

synchronous oscillation signal outputted from the oscillator in the output circuit of the master power source circuit via the third terminal to perform synchronous control of the clock signal based on the synchronous oscillation signal.

Claim 33 (Previously Presented): A multiple output power source apparatus comprising a plurality of power source circuits individually generating a plurality of DC voltages, each of the plurality of power source circuits being equipped with an independent output control circuit, wherein

each of the output control circuits respectively comprises:

a shutdown circuit that detects an abnormality of own power source circuit to output an abnormality signal to output control circuits of an other power source circuit selected from the plurality of power source circuits, and inputting an abnormality signal outputted from the output control circuit of the other power source circuit to shut down the own power source circuit when an abnormality is detected either in the own power source circuit or in the other power source circuits, each of the output control circuits being operably coupled to each other;

an output control circuit of a master power source circuit in the plurality of the power source circuits outputs a synchronous oscillation signal to a control circuit of a slave power source circuit selected from the plurality of the power source circuit; and

the output control circuit of the slave power source circuit inputs the synchronous oscillation signal outputted from the output control circuit of the master power source circuit to perform synchronous control with the control circuit of the master power source circuit based on the synchronous oscillation signal, whereby the own power source circuit and the other power source circuits simultaneously shut down and the master power source circuit and the slave power source circuit synchronously oscillate when an abnormality is detected either in the own power source circuit or in the other power source circuits.

Claim 34 (Previously Presented): The multiple output power source apparatus according to claim 33, wherein

the plurality of the power source circuits respectively comprise a converter that is driven by a switching circuit, converts an input voltage into a prescribed output voltage, and outputs the prescribed output voltage;

the output control circuit of the master power source circuit outputs the synchronous oscillation signal synchronized with the switching signal to a control circuit of the slave power source circuit; and

the control circuit of the slave power source circuit causes the switching signal to be in synchronism with the switching signal of the output control circuit of the master power source circuit based on the synchronous oscillation signal.

Claim 35 (Previously Presented): A multiple output power source apparatus comprising a plurality of power source circuits which respectively comprises a converter that is driven by a switching circuit, converts an input voltage into a prescribed output voltage, and outputs the prescribed output voltage; and an output control circuit that controls the converter, the plurality of power source circuits, individually generating a plurality of DC voltages, being connected in parallel to a single power source, wherein

each of the output control circuits comprises:

a stabilizing circuit that stabilizes the output voltage of the converter to a prescribed value by monitoring the output voltage of a converter of own power source circuit and controlling the switching signal; and

a shutdown circuit that detects an abnormality of own power source circuit to output an abnormality signal to output control circuits of an other power source circuit selected from the plurality of power source circuits, and inputting an abnormality signal outputted from the output control circuit of the other power source circuit to shut down the own power source circuit when

an abnormality is detected either in the own power source circuit or in the other power source circuits, each of the output control circuits being operably coupled to each other,

an output control circuit in a specified master power source circuit of the plurality of the power source circuits outputs via a first terminal a synchronous oscillation signal synchronized with the switching signal to an output control circuit of a slave power source circuit selected from the plurality of the power source circuit, and outputs the abnormal signal from the master power source circuit by stopping the synchronous oscillation signal outputted through the first terminal; and

the output control circuit of the slave power source circuit inputs the synchronous oscillation signal outputted from the output control circuit in the master power source circuit via a second terminal to perform synchronous control which causes the switching signal to be in synchronism with the switching signal of the output control circuit of the master power source circuit based on the synchronous oscillation signal, and outputs the abnormality signal by stopping the synchronous oscillation signal outputted through the second terminal, whereby the own power source circuit and the other power source circuit simultaneously shut down and the master power source circuit and the slave power source circuit synchronously oscillate when an abnormality is detected either in the own power source circuit or in the other power source circuits.

Claim 36 (Previously Presented): A multiple output power source apparatus comprising a plurality of power source circuits which respectively comprises a converter that is driven by a switching circuit, converts an input voltage into a prescribed output voltage, and outputs the prescribed output voltage; and an output control circuit that controls the converter, the plurality of power source circuits individually generating the plurality of DC voltages being connected in parallel to a single power source, wherein

the plurality of power source circuits respectively comprise:

a master power source circuit; and

one or a plurality of slave power source circuits, each output control circuit of the slave power source circuits being connected to the master power source circuit through a synchronous line,

an output circuit of the master power source circuit comprises:

an oscillator that generates a clock signal having a prescribed frequency and outputs a synchronous signal synchronized with the clock signal to the synchronous line;

a first stabilizing circuit that stabilizes the output voltage of the converter to a prescribed value by controlling the switching signal based on the clock signal oscillated at the oscillator;

a first shutdown circuit that detects an abnormality of the master power source circuit to output an abnormality signal to the synchronous line, detects an abnormality signal outputted to the synchronous line from the output control circuit of the slave power source circuit, and shuts down the master power source circuit when an abnormality is detected either in the master power source circuit or in the slave power source circuits, and

output control circuits of the slave power source circuits respectively comprise:

a second stabilizing circuit that stabilizes the output voltage of the converter to a prescribed value by controlling the switching signal based on the synchronous signal output to the synchronous line; and

a second shutdown circuit that detects an abnormality of the slave power source circuits to output an abnormality signal to the synchronous line, detects an abnormality signal outputted to the synchronous line from the output control circuit of the slave power source circuits, and shuts down the slave power source circuits when an abnormality is detected either in the master power source circuit or in the slave power source circuits, each of the output control circuits being operably connected to each other, whereby the own power source circuit and the other power source circuits simultaneously shut down and the master power source circuit and the slave power source circuit synchronously oscillate when an abnormality is detected either in the own power source circuit or in the other power source circuits.

Claim 37 (Previously Presented): The multiple output power source apparatus according to claim 36, wherein the master power source circuit and the slave power source circuits output the abnormality signal when the synchronous line is grounded, and

the first and second shutdown circuits measure time during which the synchronous signal is stopped and cause the power circuit to be shut down when the measured time is a prescribed time or longer.

Claim 38 (Previously Presented): The multiple output power source apparatus according to claim 36, wherein the master power source circuit and the slave power source circuits output the abnormality signal when a prescribed voltage is superposed on the synchronous line.

EVIDENCE APPENDIX

There is no evidence to submit.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings.